

Office Action Summary

Application No. 08-92,250	Applicant(s) Inoue et al
Examiner George Goudreau	Group Art Unit 1763

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

- ☒ Responsive to communication(s) filed on 4-17-00' (ie, paper #9)
- ☐ This action is FINAL.
- ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

- ☒ Claim(s) 3-14, 16-27 is/are pending in the application.
- Of the above claim(s) _____ is/are withdrawn from consideration.
- ☒ Claim(s) 5-6, 19 is/are allowed.
- ☒ Claim(s) 3-4, 7-14, 16-18, 20-27 is/are rejected.
- ☐ Claim(s) _____ is/are objected to.
- ☐ Claim(s) _____ are subject to restriction or election requirement.

Application Papers

- ☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.
- ☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.
- ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.
- ☐ The specification is objected to by the Examiner.
- ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

- ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
- ☒ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been received.
- ☐ received in Application No. (Series Code/Serial Number) _____
- ☐ received in this national stage application from the International Bureau (PCT Rule 1.7.2(a)).

*Certified copies not received: _____

Attachment(s)

- ☒ Information Disclosure Statement(s), PTO-1449, Paper No(s) 10
- ☒ Notice of Reference(s) Cited, PTO-892
- ☐ Notice of Draftsperson's Patent Drawing Review, PTO-948
- ☐ Interview Summary, PTO-413
- ☐ Notice of Informal Patent Application, PTO-152
- ☐ Other _____

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-the specific usage of a surfactant in the cmp slurry employed by the applicant to cmp planarize the insulating films which were conformably deposited onto the surface of the trench etched into the Si wafer

It would have been obvious to one skilled in the art to employ a surfactant in the cmp process used to planarize the insulating layers conformably deposited onto the surface of the trench etched into the Si wafer based upon the following. The usage of surfactants in a cmp slurry used to planarize the surface of wafer is conventional or at least well known in the semiconductor processing arts. (The examiner takes official notice in this regard.) Further, it is desirable to employ a surfactant in a cmp slurry used to planarize a wafer surface in order to desirable improve the wetting of the surface of the substrate with the cmp slurry. This enhancement of the wetting of the surface of the substrate with the cmp slurry would desirably enhance the reaction of the cmp slurry with the wafer surface which would in turn enhance the rate of cmp polishing of the substrate. It would also desirably lead to a more uniform polishing of the surface of the wafer by evening out the interaction of the wafer surface with the cmp slurry.

It would have been obvious to one skilled in the art to employ a SOG layer to form the first insulating layer deposited into the trench etched into the Si wafer in the process taught above based upon the following. The usage of SOG layers to form an insulating layer on a semiconductor wafer is conventional or at least well known in the semiconductor processing arts. (The examiner takes official notice in this regard.) Further, the usage of a SOG layer desirably provides excellent coverage of features on a semiconductor wafer relative to the usage of other

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20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103© and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

21. Claims 9-10, 12, 20-21, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shepard as applied in paragraph 17 above.

Shepard as applied in paragraph 17 above fail to disclose the following aspects of applicant claimed invention:

- the specific formation of the 1st insulating film conformably deposited into the trench etched into the Si wafer using an SOG process;
- the specific formation of a first insulating film with the specific H₂O wetting angles claimed by the applicant; and

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-Fifth, N ions are ion implanted into both the SOG layer (70), and the SiO₂ layer (60).

(The N ion implant step is conducted, however, such that the N ions are concentrated in the SiO₂ layer (60) to form a cmp polishing stop layer (50).); and

-Sixth, the ILD layers are cmp polished down to the surface of the polishing stop layer (50) in the SiO₂ layer (60).

This is discussed specifically in columns 4-5; and discussed in general in columns 1-8.

This is shown in figures 3a-3e; and shown in general in figures 1-3.

19. Claim 18 is rejected under 35 U.S.C. 102(b) as being anticipated by Yu et. al.

Yu et. al. disclose a process for planarizing the surface of a DRAM comprised of the following steps:

-First, a series of insulating, and conducting layers are formed on the surface of a Si wafer; and patterned to form structure (42).;

-Second, a TEOS layer is conformably deposited onto the surface of the wafer using a CVD process to form a SiO₂ layer.;

-Third, a patterned photo resist mask is used to selectively ion implant a portion of the top surface of the SiO₂ layer (46) with P, and B ions to form a transformed region (44) of BPSG on the surface of the SiO₂ layer (46).;

-Fourth, the resist ion implantation mask is removed from the surface of the wafer.; and

-Fifth, the wafer surface is planarized using a cmp polishing process.

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- Sixth, P ions are ion implanted into the surface of the SiO₂ layer (240');;
- Seventh, another layer of SiO₂ (240'') is conformably formed onto the surface of the wafer using a PECVD process.; and
- Eight, the insulating layers (240', and 240'') which were deposited onto the surface of the wafer are now planarized using a cmp process.

This is discussed specifically in columns 3-5; and discussed in general in columns 1-6.

This is shown in figures 4a-4c; and shown in general in figures 1-5.

18. Claims 3, 7-8, 11, 13-14, 18, 22, and 24-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Jang et. al. (5,674,784).

Jang et. al. disclose a process planarizing an interlayer dielectric layer (ILD) on the surface of a semiconductor wafer comprising the following steps:

- First, a patterned Al wiring layer (12)/ SiO₂ pad oxide layer (11) is formed on the surface of a Si wafer (10).;
- Second, a SiO₂ layer (60) is conformably formed onto the surface of the wafer using a CVD process.;
- Third, an SOG layer (70) is conformably formed onto the surface of the SiO₂ layer (60) in order to further facilitate planarizing of the ILD on the wafer surface.;
- Fourth, the SOG layer (70) is cmp polished in order to further planarize its surface prior to forming the polishing stop layer (50) using a N ion implantation step.;

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15. This action will not be made final due to the new grounds of rejection.
16. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

17. Claims 3-4, 7-8, 11, 13-14, 16, and 24-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Shepard (5,616,513).

Shepard discloses a process for forming a STI structure on a semiconductor wafer which is comprised of the following steps:

- First, a SiO₂ (210)/ Si₃N₄ (220) stack is formed on the surface of a Si wafer (200).;
- Second, a patterned photo resist etch mask is then formed on the surface of the SiO₂/Si₃N₄ stack.;
- Third, a trench is etched through the SiO₂/Si₃N₄ stack, and into the Si wafer using the patterned photo resist etch mask.;
- Fourth, the resist etch mask is stripped from the surface of the wafer.;
- Fifth, a SiO₂ layer (240') is conformably deposited onto the surface of the wafer using a PECVD process.;

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types of dielectric materials on a semiconductor wafer. The usage of a SOG layer to planarize a semiconductor wafer is also desirable based upon the ability to apply a thicker insulating coating on a semiconductor wafer than can be provided by other means such as with CVD processes.

It would have been *prima facie* obvious to form SiO₂ layers on the wafer surface in the semiconductor fabrication process taught above with any of a variety of different H₂O wetting angles including those specifically claimed by the applicant. These are all well known variables in the semiconductor fabrication arts which are known to effect the quality of the coating of one dielectric film with another dielectric film. Further, the selection of particular values for these variables would not necessitate any undue experimentation which would be indicative of a showing of unexpected results.

Alternatively, it would have been obvious to one skilled in the art to conformably form a first insulating film on the surface of the trench etched into the Si wafer in the process taught above with the specific wetting angles claimed by the applicant based upon the case law listed below.

"Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller*, 220 F. 2d 454, 105 USPQ 233, 235 (CCPA).

22. Claims 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jang et. al. as applied in paragraph 18 above.

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Jang et. al. as applied in paragraph 18 above fail to specifically disclose the usage of a surfactant such as a fatty acid based surfactant in the cmp slurry used to initially polish the surface of the SOG layer prior to conducting the ion implantation step.

It would have been obvious to one skilled in the art to add a surfactant such as a fatty acid based surfactant to the cmp slurry used to initially planarize the SOG layer in the process taught in paragraph 18 above based upon the following. The usage of surfactants such as fatty acid based surfactants in a cmp slurry used to planarize a semiconductor based material such as SOG is conventional or at least well known in the semiconductor processing arts. (The examiner takes official notice in this regard.) Further, the addition of a surfactant to a cmp slurry used to planarize an SOG layer on a wafer would have desirably had the property of improving the wetting of the SOG layer by the cmp slurry during the cmp polishing process. This in turn would have desirably improved the chemical reaction between the SOG layer, and the cmp slurry during the cmp polishing process by improving the wetting of the SOG layer with the cmp slurry. The improvement of the chemical reaction of the SOG layer with the cmp slurry would have desirably lead to an enhancement in both the rate, and the uniformity of the polishing of the SOG layer on the wafer.

23. Claims 5-6, and 19 are allowed.

24. Claims 3-4, 9-14, 16-18, and 20-25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

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In claim 7, applicant refers to a first, second, and fourth film but fails to mention the third film. This is confusing since the examiner presumes that there is a third film.;

In claim 17, applicant refers to a first, and a third film but fails to mention the second film. This is confusing since the examiner presumes that there is a second film.;

In claim 18, applicant refers to a first, and fourth film but fails to mention the second and third films. This is confusing since the examiner presumes that there are a second, and third film. (It is suggested that applicant avoid these problems by not referring to individual layers by the terms "first", "second", "third", or "fourth", but instead using names to refer to each layer based upon their function.);

In claim 3, the word "planrization" should read "planarization".; and

In line 8 of claim 8, it is unclear which insulating layer is being referred to by the phrase "said insulation film". Claim 8 is vague, and indefinite in this regard.

(The examiner has not rejected claim 17 over the prior art of record due to the fact that the examiner cannot tell exactly what applicant is trying to claim in this claim for the reasons stated above.)

25. Claim 17 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

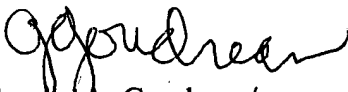
26. The examiner lined through references which were listed on the attached 1449 forms but were not supplied to the examiner by applicant. If applicant wishes for these listed references to be considered of record by the examiner, then applicant must resubmit a 1449 form listing these

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27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner George A. Goudreau whose telephone number is (703) -308-1915. The examiner can normally be reached on Monday through Friday from 9:30 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Examiner Gregory Mills, can be reached on (703) -308-1633. The appropriate fax phone number for the organization where this application or proceeding is assigned is (703) -308-3599.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) -308-0661.


George A. Goudreau/gag

Examiner AU 1763